WHAT IS CLAIMED IS:

1. A method for providing row sense and row precharge currents to a memory, comprising the steps of:

providing first current profiles for the row sense and row precharge currents during normal memory accesses; and

providing a second current profile for at least one of the row sense and row precharge currents during a memory refresh, the second current profile having less of a current spike than the first profiles.

2. A method for providing row sense current to a memory, comprising the steps of:

providing a first current profile for the row sense current during normal memory accesses; and

providing a second current profile for the row sense current during a memory refresh, the second current profile having less of a current spike than the first profile.

3. A method for providing row precharge current to a memory, comprising the steps of:

providing a first current profile for the row precharge current during normal memory accesses; and

providing a second current profile for the row precharge current during a memory refresh, the second current profile having less of a current spike than the first profile.

4. A method of refreshing a memory device, comprising the steps of: providing a sequence of bank addresses for refreshing over an interface to the memory device; and using an internal sequencer in the memory device to provide sequencing of row addresses.

5. A method of refreshing a memory device, comprising the steps of:

providing a sequence of row addresses for refreshing the memory device; and

for each row, refreshing the row in a sequence of banks before refreshing a subsequent row.

6. The method of claim 5 further comprising the steps of:

providing a sequence of bank addresses for refreshing over an interface to the memory device; and

using an internal sequencer in the memory device to provide sequencing of row addresses.

7. A method of refreshing a memory device, comprising the steps of:

simultaneously refreshing a plurality of banks.

8. A memory device comprising:

a memory array;

a plurality of sense amplifiers connected to the memory array;

a control circuit connected to the sense amplifiers, the control circuit being configured to control the sense amplifiers to:

provide first current profiles for row sense currents during normal memory accesses; and

provide second current profiles for the row sense currents during a memory refresh, the second current profiles having less of a current spike than the first profiles.

9. The memory device of claim 8 further comprising:

a plurality of sense amplifier driver transistors;

wherein the control circuit provides a drive signal to the driver transistors using a reduced slew rate for a memory refresh.

10. The memory device of claim 8 further comprising:

a plurality of sense amplifier driver transistors;

wherein the control circuit provides a drive signal to the driver transistors using a lower drive voltage for a memory refresh than for other memory operations.

11. The memory device of claim 8 further comprising:

a plurality of sense amplifier driver transistors connected in parallel;

wherein the control circuit sequentially turns on the driver transistors for a memory refresh.

12. A memory device comprising:

a memory array;

a plurality of row precharge drivers connected to the memory array;

a control circuit connected to the row precharge drivers, the control circuit being configured to control the row precharge drivers to

provide first current profiles for row precharge currents during normal memory accesses; and

provide second current profiles for the row precharge currents during a memory refresh, the second current profiles having less of a current spike than the first profiles.

13. The memory device of claim 12 further comprising:

a plurality of row precharge driver transistors;

wherein the control circuit provides a drive signal to the driver transistors using a reduced slew rate for a memory refresh.

14. The memory device of claim 12 further comprising:

a plurality of row precharge driver transistors;

wherein the control circuit provides a drive signal to the driver transistors using a lower drive voltage for a memory refresh.

15. The memory device of claim 12 further comprising:

a plurality of row precharge driver transistors connected in parallel;

wherein the control circuit sequentially turns on the driver transistors for a memory refresh.

16. A memory device comprising:

an internal sequencer configured to provide sequencing of row addresses for each of a plurality of banks in the memory device; and

an interface circuit configured to receive a sequence of bank addresses for refreshing over an interface, and provide enabling control signals to the internal sequencer.

17. A method of refreshing a memory device, comprising the steps of:

at one of a plurality of clock rates, selected in accordance with a device configuration signal:

internally generating a sequence of row addresses for refreshing the memory device; and

refreshing a row of the memory device associated with a currently generated row address.

18. The method of claim 17 wherein the device configuration signal is set by determining a worst case memory cell hold time for memory cells in the memory device and setting the device configuration signal in accordance with the determined worst case memory cell hold time.

19. A memory device, comprising:

a memory array;

a plurality of sense amplifiers connected to the memory array; and

a control circuit connected to the sense amplifiers, the control circuit being configured to control the sense amplifiers to refresh memory cells in the memory array, one row at a time, at one of a plurality of clock rates, selected in accordance with a device configuration signal.

20. The memory device of claim 19 wherein the control circuit includes a row address counter, and the device configuration signal is a permanently set signal, having one of a plurality number of predefined values, that determines which of a like plurality of clock signals are used to increment the row address counter and to initiate a row refresh operation.